TECHNICAL DATA

LeCroy
RESEARCH SYSTEMS

CAMAC Model 2341A

16-Channel Coincidence Register

NEW!
Inputs respond to signals as low as −100 mV!

- **16 channels in single-width module** . . . less space than that required by other designs.
- **Summing outputs** provide fast trigger capability . . . organized in two groups of eight registers for use in multiplicity decisions.
- **Fast clear input** . . . permits use of loose pretrigger (so summing output can participate in final logic decision) without deadtime generating dataway clearing operation.
- **Narrow coincidence widths** . . . High speed design permits coincidence width as narrow as 1 nsec.
- **Input double-pulse resolution <10 nsec** . . . assures high efficiency even in high count rate applications.
- **Accepts input amplitudes as low as −100 mV** . . . permits triggering even after substantial attenuation from long cable delays.

The LeCroy Model 2341A Coincidence Register ("pattern unit") offers fast storage functions in computer-compatible CAMAC standard packaging. The integrated circuit design affords high density packaging, permitting 16 complete channels in one CAMAC single-width module.

The 2341A operates from standard NIM logic levels. The logic channels, which seek a coincidence between each input and a common fast gate input, employ MECL III integrated circuits and provide coincidence resolving times under 2 nsec. Logical "1" data levels, representing the time coincidence between the common gate and the 16 inputs, are stored in a 16-bit fast buffer register for later readout under CAMAC commands. The facility of performing majority logic is provided by two rear-panel summing outputs which are each driven by 8 logic channels. The output current of the summing circuit is proportional, in increments of 4 mA per register bit, to the number of coincidences stored in the register. Bridged high impedance outputs permit cascading any number of summing outputs. Other operating features include a front-panel clear input which responds to negative logic levels and a built-in test mode.

The Model 2341A Coincidence Register is a member of LeCroy's CAMAC Series, a growing line of instruments which combine high performance with the flexibility and computer compatibility of the CAMAC standard.

November 1977

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, NEW YORK 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPONE: (914) 425-2000

SPECIFICATIONS
CAMAC Model 2341A
16-CHANNEL COINCIDENCE REGISTER

INPUT CHARACTERISTICS

Inputs:	16, Lemo connectors; impedance 50 Ω ± 5%; direct-coupled; protected to ±10 volts for inputs <1 μsec; reflections <10% for 2 nsec risetime.
Required Input Level:	Adjustable from −100 mV to −1.0 V with rear-panel potentiometer.
Double Pulse Resolution:	10 nsec max.; 8 nsec typical.
Gate Input:	One; Lemo connector; 50 Ω impedance; −600 mV or greater enables; minimum duration at full logic level (−750 mV), 2.0 nsec; protected to ±100 V. Should precede inputs by at least 3 nsec.
Clear Input:	One, Lemo connector: −600 mV or greater, 50 Ω impedance; minimum duration, 10 nsec; protected to ±100 V. 10 nsec settling time after clear.

OUTPUT CHARACTERISTICS

Data Readout:	CAMAC function and address commands gate the 16 binary bits on to the 2^0 to 12^{15} CAMAC dataway bus lines; logical 1, ≤0.5 volts (0 to 16 mA); logical 0, open circuit (≤ 100 μA at 5.5 volts).
Summing Outputs:	2; one pair of high impedance bridged connectors for each set of 8 inputs; 4 mA ± 3% is presented for each register latched; maximum output into 25 Ω, −1 volt for single or cascaded units (corresponds to 10 set registers); risetime, 4 nsec (increasing slightly for multiple levels); delay of leading edge of summing output from leading edge of input, 20 nsec.

GENERAL

Coincidence Width:	1 nsec up, determined by input and gate pulse durations.
CAMAC Commands:	Z or C: Clears register, requires S2. I: Gate Input is inhibited for duration of CAMAC inhibit commands. Q: A Q=1 response is generated in recognition of an F(0), F(2), F(9), or F(25) for a valid N and A(0), but there will be no response (Q=0) under any other condition. X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated.
CAMAC Function Codes:	F(0): Read group 1 register; requires N and A(0). F(2): Read and Clear group 1 register; requires N, A(0), and S2. F(9): Clear Group 1 register; requires N, A(0), and S2. F(25): Increment (test mode latches all channels); requires N and S2.
Packaging:	CAMAC single-width module. Conforms to ESONE Report EUR 4100 or IEEE #583 standards.
Power Requirements:	+6 V at 500 mA −6 V at 800 mA −24 V at 65 mA